Reference Design of CGH40006S
Low Noise Amplifier Demonstrator Circuit

Introduction

This low noise amplifier circuit was developed using a CGH40006S GaN HEMT transistor as a means of demonstrating the wide bandwidth low noise performance and ruggedness of the device. This application note describes the typical performance that has been achieved and that which can be expected when evaluating the demonstrators. Details of the circuit are included for further understanding of the topology and all necessary information has been provided to aid reproduction of the amplifier.

Features

- Demonstrator of performance over 225 MHz - 2 GHz
- 17 dB Small Signal Gain
- >50 % Power Added Efficiency
- <3 dB Noise Figure

PN: CGH40006S-LNA-KIT

Application Note

Basic Amplifier Specification

Maximum Ratings for Evaluation of Demonstrator @ 25°C

Parameter	Test Conditions	Units	Minimum	Maximum
Gate-to-Source Voltage	—	V	-10	+2
Frequency	—	GHz	0.225	2
Input Power Level	CW No Degradation CW Device Failure Pulsed 300 µs 10% Duty Cycle, No Degradation Pulsed 300 µs 10% Duty Cycle, Device Failure	dBm	—	39 42 44 46
Operating Junction Temperature	—	˚C	—	+175
Case Temperature	—	˚C	-40	+150

Typical Low Noise Amplifier Demonstrator Performance

Characteristics	Test Conditions	Units	Frequency			
			225 MHz	500 MHz	1000 MHz	2000 MHz
Small Signal Gain	—	dB	18.5	18.0	17.0	17.5
Input Return Loss	—	dB	-12.5	-9	-7	-6
Power Gain	P_{IN} = 25 dBm	dB	13.7	13.5	13.2	12.8
Power Added Efficiency	P_{IN} = 25 dBm	%	57.5	57.0	50.0	40.0
Nose Figure	—	dB	1.75	2.1	2.5	3.15

Note 1: IDQ = 50 mA
Note 2: Individual device characteristics are as per CGH40006S datasheet
Note 3: VGS has been selected for best noise figure / efficiency tradeoff

Typical Circuit Bias Conditions

Circuit Element	Bias Voltage	Quiescent Bias Circuit
Gate Bias	-3	50 mA
Drain Voltage	+28	Note: Gate bias must be applied before the drain bias is activated

Application Note

Details of the CGH40006S Demonstrator Circuit

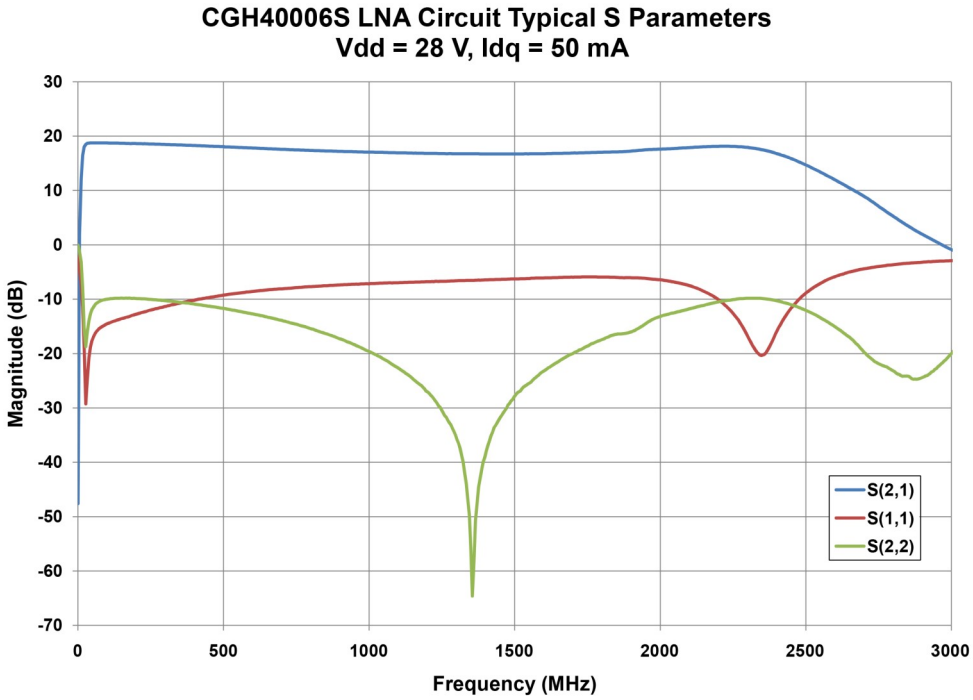

Figure 1 -CGH40006S LNA Circuit - Typical S-parameters

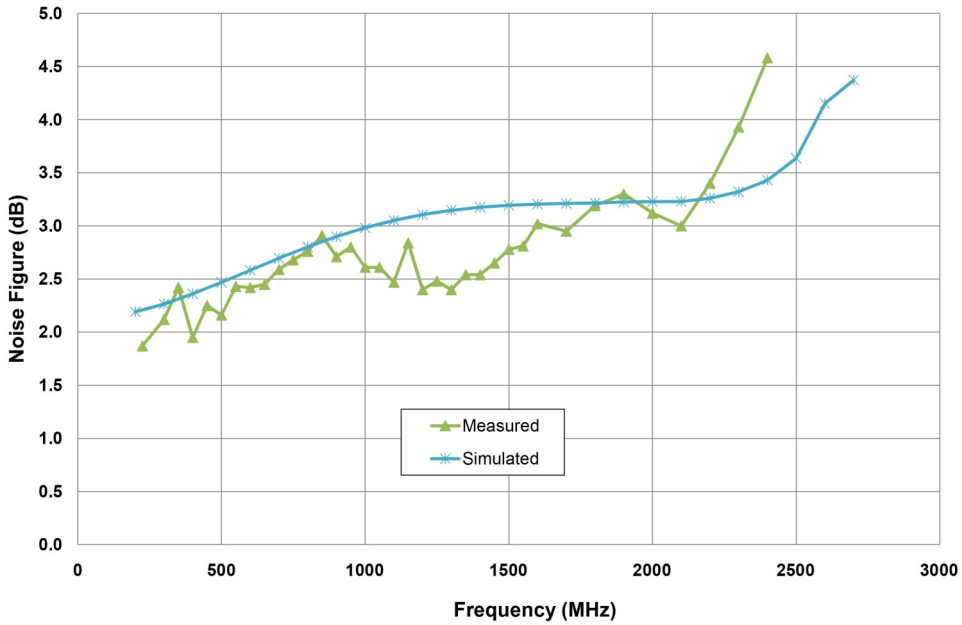

Figure 2 -CGH40006S LNA Circuit - Noise Figure vs. Frequency

Application Note

Details of the CGH40006S Demonstrator Circuit

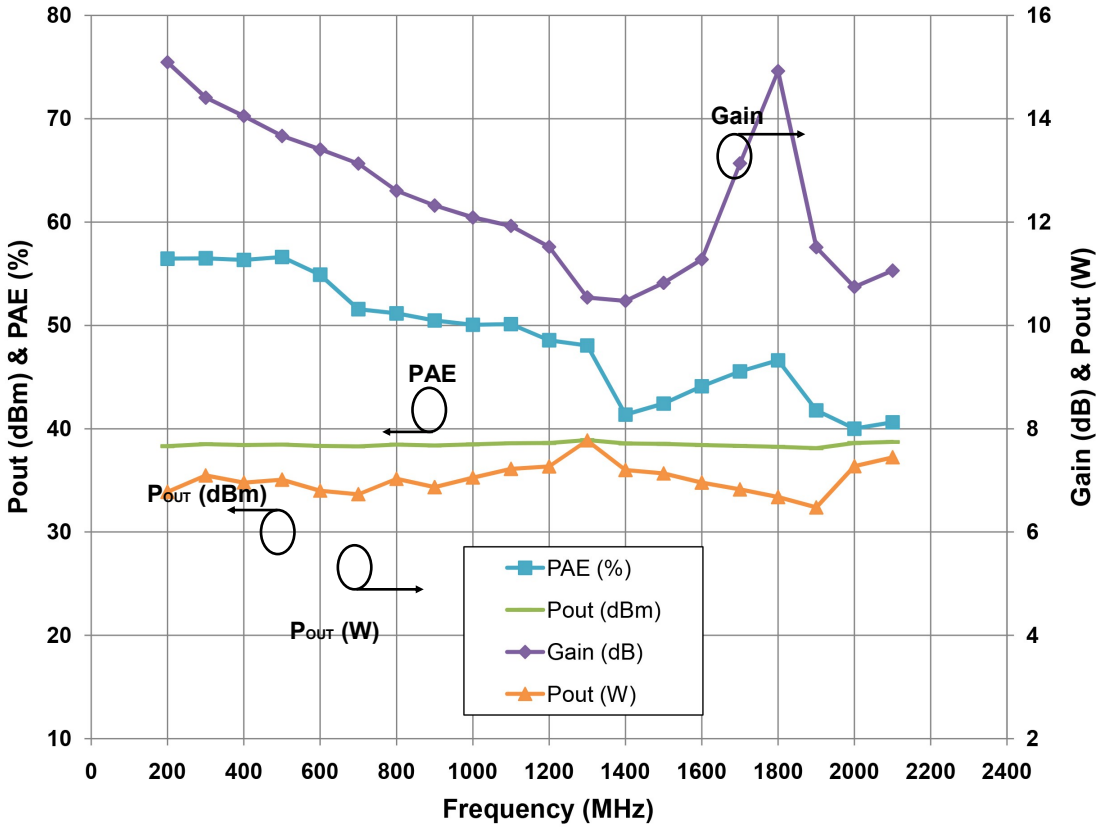

Figure 3 -CGH40006S LNA Circuit - P_{SAT}, PAE and Power Gain vs. Frequency

Application Note

Details of the CGH40006S LNA Kit Demonstrator Circuit

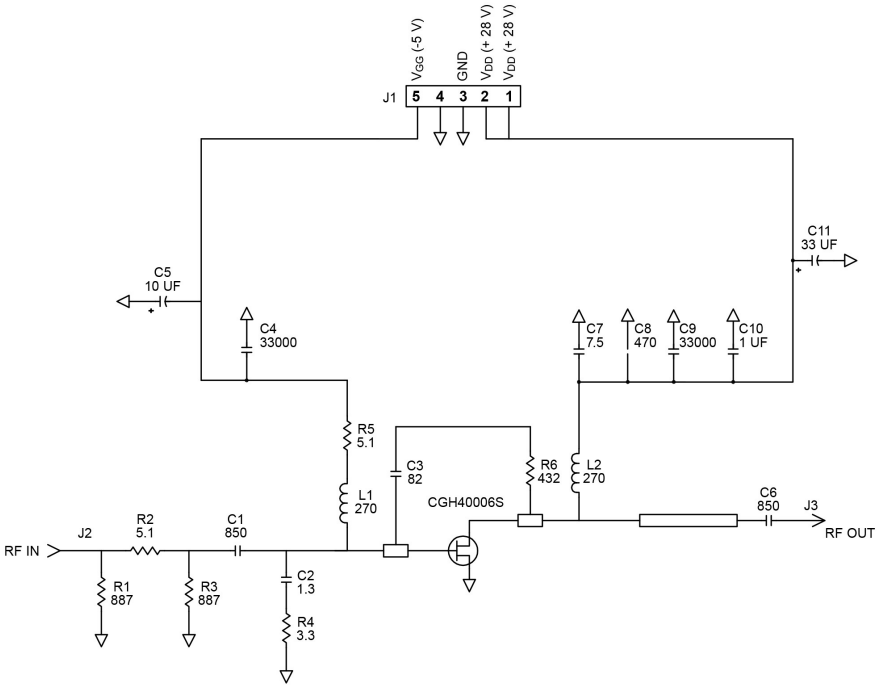

Figure 4 - Schematic of CGH40006S-LNA-KIT Demonstrator Circuit

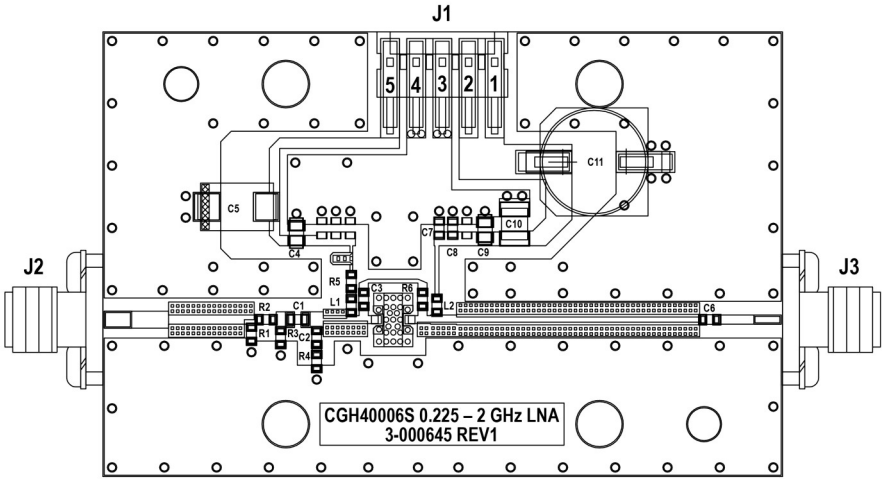

Figure 5 - CGH40006S-LNA-KIT Demonstrator Printed Circuit Board Assembly

Application Note

Details of the CGH40006S LNA Kit Demonstrator Circuit

CGH40006S LNA Kit Demonstrator Circuit Bill of Materials

Reference Designator	Description	Quantity
R1, R3	RES, 1/16W, 0603, 1%, 887 Ohms	2
R2, R5	RES, 1/16W, 0603, 1%, 5.1 Ohms	2
R4	RES, 1/16W, 0603, 1%, 3.3 Ohms	1
R6	RES, 1/16W, 0603, 1%, 432 Ohms	1
C1, C6	CAP, DC BLOCK, MULTI-LAYER, 0603, 850pF	2
C2	CAP, 1.3pF, +/-0.1pF, 0603, ATC	1
C3	CAP, 82.0pF, +/-5%, 0603, ATC	1
C5	CAP 10uF, 16V, TANTALUM	1
C7	CAP, 7.5pF, +/-0.1pF, 0603, ATC	1
C8	CAP, 470pF, 5%, 100V, 0603	1
C9	CAP, 33000pF, 0805, 100V, X7R	1
C10	CAP, 1.0uF, 100V, 10%, X7R, 1210	1
C11	CAP, 33 uF, 20%, G CASE	1
L1, L2	INDUCTOR, SMT, 0603, 270nH, 5%, RoHS COMPLIANT	2
J1	HEADER RT>PLZ .1CEN LK 5POS	1
J2, J3	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST	2
	PCB, RO4350B, 20 MIL THK, CGH40006S 225 MHz - 2 GHz LNA |APPLICATION CIRCUIT	1
	2-56 SOC HD SCREW 1/4 SS	4
	#2 SPLIT LOCKWASHER SS	4

Conclusion

This application note has shown the performance advantages of using discrete GaN HEMT transistors for low noise amplifiers. The reference design here shows that it is possible to achieve wide bandwidths, high power and efficiency whilst maintaining low noise and is able to withstand CW input power of 5 W with no degradation. As this transistor is unmatched performance can be replicated at other frequency bands. This reference design was generated with first pass success using large signal models, which are available on request.

Application Note